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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APR 18 2005
PATENT & TRADEMARK OFFICE
In re U.S. Patent No. 6,830,964 B1)
MEARS ET AL.)
Issued: DECEMBER 14, 2004)
For: METHOD FOR MAKING SEMICONDUCTOR)
DEVICE INCLUDING BAND-)
ENGINEERED SUPERLATTICE)

REQUEST FOR CERTIFICATE OF CORRECTION OF
APPLICANT'S MISTAKE UNDER RULE 1.323

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of Rule 1.323 of the Rules of Practice, the Patent Office is respectfully requested to correct matters in the above-identified patent in accordance with the Certificate of Correction Form PTO-1050 attached hereto.

The Patent Office is requested to issue a Certificate of Correction on the above-referenced Patent Document, and to place such a Certificate of Correction in the file, so that such will appear on any copies of the patent which are ordered in the future.

The corrections being made are of consequence to provide the proper recitation on the cover page, in the drawings and specification. Several of the mistakes occurred in good faith and are not the fault of the Patent and Trademark Office. However, two printing errors of the Patent Office are also being corrected. No new matter is added by these corrections.

04/19/2005 NGUYEN 00000007 6830964
01 FC:1011 100.00 UP

In re Patent of
MEARS ET AL.
Patent No. 6,830,964 B1
Issued: DECEMBER 14, 2004

Authorization is given to charge the requisite fee as set forth in 37 CFR § 1.20(a) in the amount of \$100.00 to the credit card listed on the attached credit card payment form PTO-2038. The Commissioner is authorized to charge or credit any discrepancies in fee amounts to Deposit Account 01-0484.

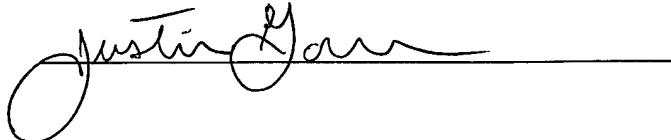
Respectfully submitted,



CHRISTOPHER F. REGAN
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Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Ave., Suite 1401
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, on this 15th day of April, 2005.



UNITED STATES PATENT AND TRADEMARK OFFICE

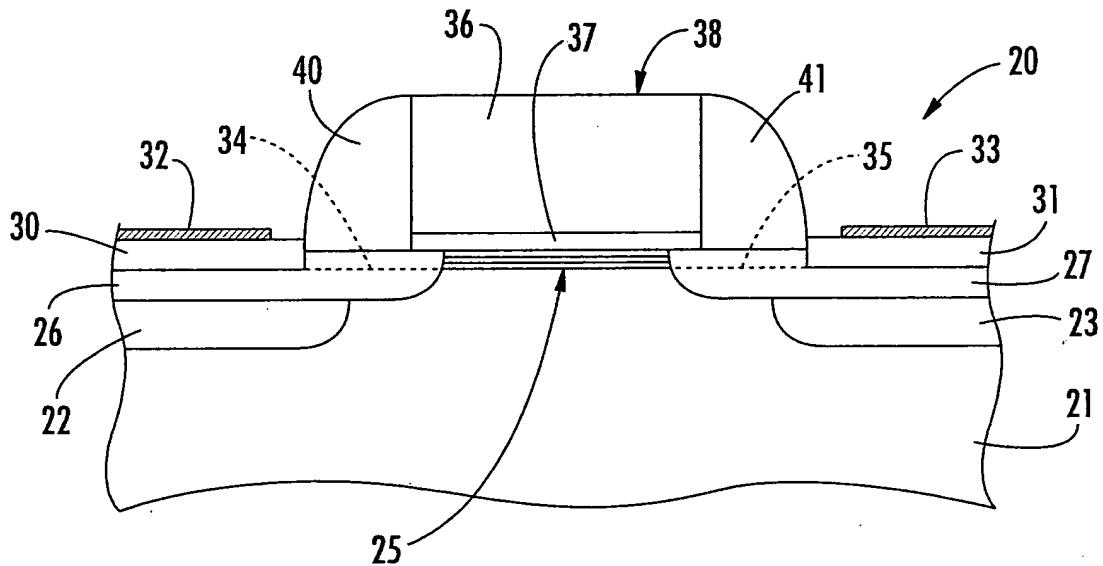
CERTIFICATE OF CORRECTION

PATENT NO.	:	6,830,964 B1
DATED	:	December 14, 2004
INVENTOR(S)	:	Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

Cover Page,
Drawing

Delete: FIG. 1
Insert: New FIG. 1



MAILING ADDRESS OF SENDER:

Christopher F. Regan

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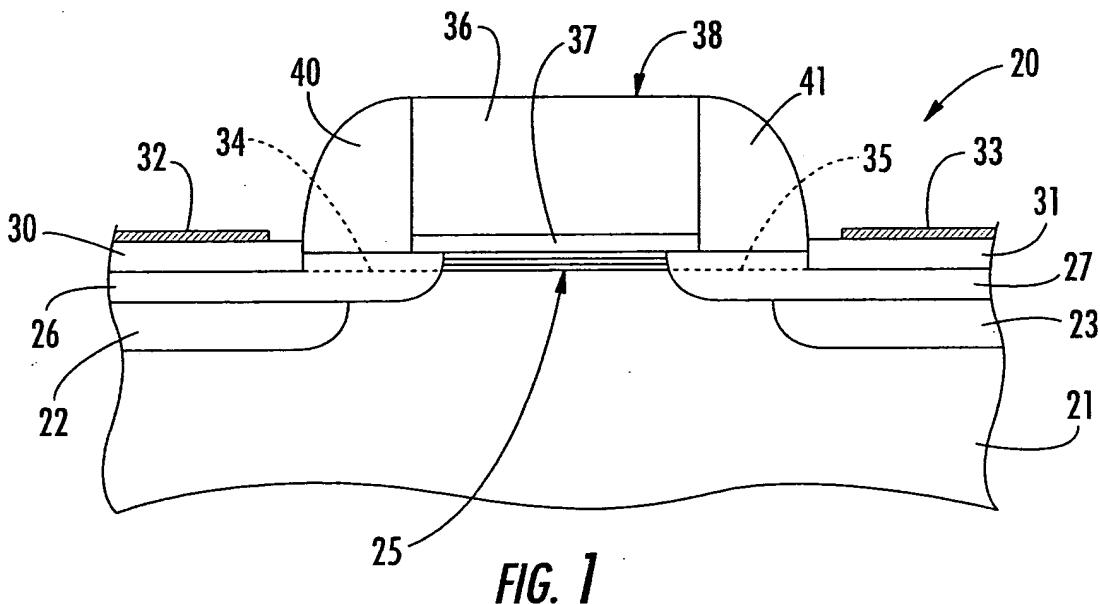
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In the Drawings

Delete: FIG. 1

Insert: New FIG. 1



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Column 1, Line 44 Delete: "on a binary"
 Insert: --on binary--

Column 2, Line 2 Delete: "in a silicon"
 Insert: --in silicon--

Column 2, Line 3 Delete: "electromuminescence"
 Insert: --electroluminescence--

Column 2, Line 62 Delete: "superlattice and has"
 Insert: --superlattice has--

Column 3, Line 49 Delete: "Si/o"
 Insert: --Si/O--

Column 4, Line 32 Delete:

$$\mathbf{M}_{k,i,j}^1(E_F, T) = \frac{- \sum_{E < E_F \text{ B.Z.}} \int (\nabla_{\mathbf{k}} E(\mathbf{k}, n))_i (\nabla_{\mathbf{k}} E(\mathbf{k}, n))_j \frac{\partial f(E(\mathbf{k}, n), E_F, T)}{\partial E} d^3\mathbf{k}}{\sum_{E < E_F \text{ B.Z.}} \int (1 - f(E(\mathbf{k}, n), E_F, T)) d^3\mathbf{k}}$$

Insert:

$$\mathbf{M}_{h,i,j}^1(E_F, T) = \frac{- \sum_{E < E_F \text{ B.Z.}} \int (\nabla_{\mathbf{k}} E(\mathbf{k}, n))_i (\nabla_{\mathbf{k}} E(\mathbf{k}, n))_j \frac{\partial f(E(\mathbf{k}, n), E_F, T)}{\partial E} d^3\mathbf{k}}{\sum_{E < E_F \text{ B.Z.}} \int (1 - f(E(\mathbf{k}, n), E_F, T)) d^3\mathbf{k}}$$

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Column 5, Line 13	Delete: "gate 35" Insert: --gate 38--
Column 5, Line 61	Delete: "gate 35" Insert: --gate 38--
Column 7, Line 63	Delete: "from the both" Insert: --from both--
Column 9, Lines 44-46	Delete: "In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer."
Column 9, Line 59	Delete: "also formed" Insert: --also be formed--

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